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QUERY CONTROL FORM			RTIS USE ONLY	
Application No. 10/611,739	Prepared by	AMW	Tracking Number	0599/1768
Examiner-GAU 1e-2818	Date	9/17/04	Week Date	8/9/04
	No. of queries	3	IFW (RUN)	

JACKET			
a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other

SPECIFICATION

a. Page Missing
b. Text Continuity
c. Holes through Data
d. Other Missing Text
e. Illegible Text
f. Duplicate Text
g. Brief Description
h. Sequence Listing
i. Appendix
j. Amendments
k. Other

CLAIMS

a. Claim(s) Missing
b. Improper Dependency
c. Duplicate Numbers
d. Incorrect Numbering
e. Index Disagrees
f. Punctuation
g. Amendments
h. Bracketing
i. Missing Text
j. Duplicate Text
k. Other

MESSAGE (1) Improper Dependency: in the claim set dated 7-1-04, Claim 34 (renumbered claim 7) is dependent upon larger claim 42 (renumbered claim 15). Please advise/correct claim dependency.
(2) PTO-1449 (2 pages): Please either initial or line through citations (copies provided for reference).
(3) Print FIG. shown in IFW form is 12A-12E (total of Five) - exceeded the four limit. Please verify.

Thank You,
initials AMW

RESPONSE

initials

forming a p transistor and an n transistor in the heterostructure, wherein the strained layer comprises a channel of at least one of the transistors, the transistors being interconnected in a CMOS circuit.

6 ~~33.~~ The method of claim 5 ~~32~~ wherein the heterostructure further comprises an insulating layer below the strained layer.

7 ~~34.~~ The method of claim 15 ~~42~~ wherein the heterostructure further comprises a SiGe graded buffer layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate.

8 ~~35.~~ The method of claim 5 ~~32~~ wherein the strained layer comprises Si.

9 ~~36.~~ The method of claim 5 ~~32~~ wherein $0.1 < x < 0.5$.

10 ~~37.~~ The method of claim 5 ~~32~~ wherein the CMOS circuit comprises a logic gate.

11 ~~38.~~ The method of claim 10 ~~37~~ wherein the logic gate is a NOR gate.

FORM PTO - 1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY DOCKET NO.: ASC-044C1 APPLICANT(S): Fitzgerald *et al.* SERIAL NO.: 10/611,739 FILING DATE: July 1, 2003 GROUP: 2818

PATENT & TRADEMARK OFFICE AUG 19 2004 IPE SC110

U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A140	4,987,462	01/22/1991	Kim *et al.*	357	22	01/06/1987
	A141	5,240,876	08/31/1993	Gaul *et al.*	437	131	06/01/1992
	A142	5,424,243	06/13/1995	Takasaki	437	132	09/09/1994
	A143	5,572,043	11/05/1996	Shimizu *et al.*	257	18	05/15/1995
	A144	5,786,614	07/28/1998	Chuang *et al.*	257	318	04/08/1997
	A145	6,352,909	03/05/2002	Usenko	438	458	05/26/2000
	A146	6,524,935	02/25/2003	Canaperi et al.	438	478	09/29/2000
	A147	6,646,322	11/11/2003	Fitzgerald	257	531	07/16/2001
	A148	6,677,192	01/13/2004	Fitzgerald	438	172	07/16/2001
	A149	6,703,144	03/09/2004	Fitzgerald	428	641	03/18/2003
	A150	6,703,688	03/09/2004	Fitzgerald	257	616	7/16/2001
	A151	6,709,903	03/23/2004	Christiansen	438	149	04/30/2003

FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B44	2004/006327	01/15/2004	WO					Y
	B45	2004/0006311	01/15/2004	WO					Y
	B46	61-141116	06/28/1986	JP					Y (abstract only)
	B47	2-210816	08/22/1990	JP					Y (abstract only)
	B48	3-036717	02/18/1991	JP					Y

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)
	C92 Grillot *et al.*, "Acceptor diffusion and segregation in $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ heterostructures," Journal of Applied Physics, Vol. 91, No. 8 (2002), pp. 4891-4899.
	C93 Halsall *et al.*, "Electron diffraction and Raman studies of the effect of substrate misorientation on ordering in the AlGaInP system," Journal of Applied Physics, Vol. 85, No. 1 (1999), pp. 199-202.
	C94 Hsu *et al.*, "Surface morphology of related Ge_xSi_{1-x} films," Appl. Phys. Lett., Vol. 61, No. 11 (1992), pp. 1293-1295

EXAMINER	DATE CONSIDERED

FORM PTO - 1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY DOCKET NO.: ASC-044C1 APPLICANT(S): Fitzgerald *et al.* SERIAL NO.: 10/611,739 FILING DATE: July 1, 2003 GROUP: 2818

U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A152	6,713,326	03/30/2004	Cheng *et al.*	438	149	03/04/2003
	A153	6,723,661	04/24/2003	Fitzgerald	438	763	07/16/2001
	A154	6,737,670	05/18/2004	Cheng *et al.*	257	19	03/07/2003
	A155	6,750,130	06/15/2004	Fitzgerald	438	607	01/07/2001
	A156	2002/0084000	07/04/2002	Fitzgerald	148	33.2	12/17/2001
	A157	2003/0034529	02/20/2003	Fitzgerald *et al.*	257	369	10/08/2002
	A158	2003/0102498	06/05/2003	Braithwaite *et al.*	257	288	09/24/2002
	A159	2003/0199126	10/23/2003	Chu *et al.*	438	149	04/23/2002
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	A161	2003/0215990	11/20/2003	Fitzgerald *et al.*	438	172	03/14/2003
	A162	2003/0218189	11/27/2003	Christiansen	257	200	11/19/2002
	A163	2003/0227057	12/1/2003	Lochtefeld *et al.*	257	347	10/04/2002
	A164	2004/0005740	01/01/2004	Lochtefeld *et al.*	438	149	06/06/2003
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	A168	2004/0075149	04/22/2004	Fitzgerald *et al.*	257	369	07/23/2003

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)
	C95 IBM Technical Disclosure Bulletin, Volume 32, No. 8A, January 1990, "Optimal Growth Technique and Structure for Strain Relaxation of Si-Ge Layers on Si Substrates", pp. 330-331.
	C96 Ota, Y. et al., "Application of heterojunction FET to power amplifier for cellular telephone," Electronics Letters, Vol. 30 No. 11 (May 26, 1994) pp. 906-907.
	C97 Sakaguchi et al., "ELTRAN® by Splitting Porous Si Layers," Proc. 195th Int. SOI Symposium, Vol. 99-3, Electrochemical Society (1999) pp. 117-121.

EXAMINER	DATE CONSIDERED

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